Appl. No. 10/828,755 Amendment dated May 8, 2007 Reply to Restriction of February 8, 2007

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-32 (Canceled)

Claim 33(Currently amended): A probe card assembly comprising:

a serial signal interface configured to connect to a test system controller;

a serial digital to analog converter configured to serially receive through the serial signal interface digital first test signals in serial from the test system controller, that are to be distributed to test probes of the probe eard in analog form; the digital to analog converter configured to convert the first test signals to parallel, and [[to]] provide the first test signals to [[the]] a plurality of first test probes in analog form, wherein the first test probes are configured to contact ones of a plurality of electronic devices under test; and

a parallel analog to digital converter configured to receive analog response signals in parallel from second test probes configured to contact ones of the electronic devices under test, convert the response signals to serial, and provide the response signals through the serial signal interface in digital form to the test system controller.

Claim 34 (Canceled)

Claim 35 (Currently amended): The probe card assembly of elaim 34 claim 33 comprising:

a space transformer supporting the first test probes and the second test probes;

at least one daughter card; and

a base PCB electrically interconnected with the space transformer and the at least one daughter card, wherein the serial digital to analog converter and the <u>parallel</u> analog to digital converter are each provided on at least one of the space transformer, the base PCB, and the at least one daughter card.

Claims 36 and 37 (Canceled)

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Claim 38 (New): The probe card assembly of claim 34 further comprising a signal connection configured to receive a second test signal from the test system controller and distribute the second test signal to a plurality of third test probes, wherein each of the third test probes is configured to contact a different one of the devices under test.

Claim 39 (New): The probe card assembly of claim 38 further comprising a switching circuit configured to select for connection to the test system controller any one of a plurality of fourth test probes configured to contact a different one of the devices under test.

Claim 40 (New): The probe card assembly of claim 33 further comprising a parallel signal interface configured to receive in parallel from the test system controller third test signals.